UNCOMPRESSED IP MULTIMEDIA DATA TRANSMISSION AND SWITCHING

BACKGROUND OF THE INVENTION

1. Field of Invention

5

The present invention is directed to an apparatus and method for transmitting, receiving, and switching multimedia across an Ethernet network.

2. Description of Related Art

10   Presently, audio and video are transmitted over various mediums for various purposes. These purposes include security transmissions, class lecture transmissions (distance learning), business seminar transmissions, surgical procedure transmissions, video conferencing transmissions, and the like. For example, security cameras are stationed at various remote locations in a building. The security video from the cameras

15   is transmitted over dedicated lines and switches to a security station to monitor activity at the remote locations. Quite often the buildings having such security systems also have local area data networks such as Ethernet networks for transmitting data. Unfortunately, two separate systems must be used for the security and data network systems because of problems encountered in combining the systems.

20
In particular, security video is time sensitive and encounters unacceptable delays when transmitted on a data network. Additionally, data networks do not provide adequate bandwidth for transmitting uncompressed real time continuous video. Thus, the transmission of video across a data network requires extensive compression.

25   Unfortunately, such compression is slow, complex, and/or prohibitively expensive for security systems, or the like. Furthermore, data networks do not prioritize video data. Therefore, the video data is often broken up and suffers considerable delays. Similar problems are encountered in the transmission of lectures, seminars, video conferencing, and other like real time video transmissions. Thus, independent networks must be

maintained for uncompressed real time continuous video transmission and for data transmission because combining the transmissions is ineffective and/or cost prohibitive.

SUMMARY OF THE INVENTION

5

The present invention provides a method and apparatus for transmitting continuous video across an Ethernet network. The Ethernet network in this patent includes Fast Ethernet, (100Mb/s) or higher, such as Gigabit Ethernet (Gb/s), 10 Gigabit Ethernet (10 Gb/s), and the like. The method includes allocating a portion of an Ethernet

10 bandwidth for channel allocation, receiving a multimedia signal, assigning a channel allocation priority to the multimedia signal, transmitting data including the channel allocation priority in the allocated portion of the Ethernet bandwidth, performing video predictive coding on the multimedia signal to create a video predictive coded multimedia signal, and transmitting the video predictive coded multimedia signal over the network in

15 real time. The multimedia signal comprises a composite video signal.

The transmitting step further includes transmitting a data packet including a header and a payload, wherein the header includes the address of a master switch and the payload includes the channel allocation priority. Additionally, the performing step

20 further includes delaying a first line of the multimedia signal, and subtracting a second line of the multimedia signal from the delayed first line to create the video predictive coded multimedia signal. The method also includes receiving a video predictive coded multimedia signal from the network, performing video predictive decoding on the video predictive coded multimedia signal to create a multimedia signal, and outputting the

25 multimedia signal concurrently with the performing step.

According to another embodiment, the apparatus includes a video input that receives a video signal, a video predictive coding module coupled to the video input, and a network interface coupled to the video predictive coding module and coupled to the

30 network. The video predictive coding module performs video predictive coding on the

2

video signal in real time to create a video predictive coded signal, and the network interface transmits the video predictive coded signal across a network in real time.

The network includes an Ethernet network, such as a Fast Ethernet network or higher, and the video signal comprises a composite video signal. The video predictive coding module includes a delay module coupled to the video input, and a subtraction module coupled to the delay module. The subtraction module subtracts a subsequent line of the video signal from a delayed line of the video signal.

The delay module includes a line buffer that delays a line of the video signal to create the delayed line of the video signal and a timing control module coupled to the video input and coupled to the video predictive coding module. This timing control module controls the timing of the video predictive coding module.

In addition, the apparatus includes a channel allocation module which reserves a channel of the Ethernet network for transmitting the video predictive coded signal according to the priority of the video predictive coded signal. The apparatus also includes an analog to digital converter that converts an input video signal into a digitized video signal. The video predictive coded signal includes at least one line comprising a plurality of pixels.

According to another embodiment, the invention provides an apparatus for receiving video including a network interface that receives a video predictive coded signal from a network, a video predictive decoding module coupled to the network interface, which performs video predictive decoding on the video predictive coded signal in real time to create a video predictive decoded signal, and a video output coupled to the video predictive decoding module. The video output outputs the video predictive decoded signal in real time. The network comprises an Ethernet network and the video signal comprises a composite video signal.

In addition, the video predictive decoding module comprises a subtraction module coupled to the network interface, and a delay module coupled to the subtraction module. This subtraction module subtracts a subsequent line of the video predictive coded signal from a line of the video predictive decoded signal delayed by the delay module. The delay module includes a line buffer which delays a line of the video predictive decoded signal to create a delayed line of the video predictive decoded signal.

The apparatus includes a timing control module coupled to the video output and coupled to the video predictive decoding module, wherein the timing control module controls the timing of the video output. The timing control module includes a clock generation module coupled to the video predictive decoding module, and a memory control module coupled to the video predictive decoding module.

The apparatus further includes a channel allocation module that reserves a channel of the Ethernet network for transmitting the video predictive coded signal according to a priority of the video predictive coded signal. The apparatus additionally includes a digital to analog converter that converts the video predictive decoded signal into an output video signal. The video predictive coded signal comprises at least one line including a plurality of pixels.

According to another embodiment, the present invention provides a method of transmitting multimedia data over a network including receiving a multimedia signal, performing video predictive coding on the multimedia signal to create a video predictive coded multimedia signal, and transmitting the video predictive coded multimedia signal over the network substantially concurrently with the performing step. The network is an Ethernet network and the multimedia signal is a composite video signal.

The method also includes reserving a portion of an Ethernet bandwidth for channel allocation, assigning a channel allocation priority to the multimedia signal, and reserving a channel path for the multimedia signal. In addition, the performing step includes delaying a first line of the multimedia signal, and subtracting a second line of the

multimedia signal from the first line of the multimedia signal to create the video predictive coded multimedia signal.

The method further involves extracting a synchronization signal from the multimedia signal. The performing step performs video predictive coding in synchronization with the synchronization signal. Additionally, the method includes extracting a synchronization signal from the multimedia signal, converting the multimedia signal from analog to digital in synchronization with the synchronization signal to create a digital multimedia signal and buffering the digital multimedia signal in synchronization with the synchronization signal.

The method of receiving multimedia data from a network includes receiving a video predictive coded multimedia signal from the network, performing video predictive decoding on the video predictive coded multimedia signal to create a multimedia signal, and outputting the multimedia signal substantially concurrently with the performing step. The network is an Ethernet network and the multimedia signal is a composite video signal. The receiving step further includes receiving the video predictive coded multimedia signal from a reserved channel path of the Ethernet network. The performing step further comprises delaying a first line of a video predictive decoded multimedia signal, and subtracting a second line of the video predictive coded multimedia signal from the delayed first line of the video predictive decoded multimedia signal to create the multimedia signal.

The method further includes extracting a synchronization signal from the video predictive coded multimedia signal, where the outputting step outputs the multimedia signal in synchronization with the synchronization signal. The method also includes extracting a synchronization signal while performing the video predictive decoding, buffering the multimedia signal in synchronization with the synchronization signal, and converting the multimedia signal from digital to analog in synchronization with the synchronization signal.

According to another embodiment, the present invention provides a method for transmitting and switching multimedia data over a network by setting a portion of an Ethernet bandwidth for channel allocation, receiving a composite multimedia signal that has an assigned channel allocation priority, and reserving a channel path for the

5   composite multimedia signal. The network comprises an Ethernet network, such as a Fast Ethernet or Gigabit Ethernet network. The reserving step includes reserving a very small portion of the Ethernet bandwidth for channel allocation. The method also incorporates receiving a second multimedia signal and blocking the second multimedia signal. The method additionally includes receiving a second composite multimedia

10   signal, overriding the reserved channel path, and reserving a channel path for the second composite multimedia signal. The method also includes receiving a packet, the packet including a header addressed to a master switch, and a payload including channel allocation priority data. The multimedia signal comprises a video predictive coded composite video signal.

15

Thus, the present invention provides for the transmission of time sensitive audio/video transmission across a network. For example, a composite 7 MHz video transmission requires 8 bits per pixel to maintain 256 levels. This transmission requires over 140 Mb/s which is prohibitive on a Fast Ethernet network which only provides a

20   bandwidth of 100Mb/s. The video predictive coding reduces the pixel data down to approximately 4 bits per pixel while maintaining the 256 levels. Accordingly, the transmission of the resulting video only requires a bandwidth of approximately 70-80 Mb/s. Additionally, the present invention provides for dedicated audio/video channel allocation for high priority transmissions. Therefore, the present invention solves the

25   time sensitivity problems associated with transmitting time sensitive, real time, and continuous data across a Fast Ethernet or faster Ethernet network (such as a Gigabit or 10 Gigabit Ethernet network). Accordingly, a video signal is received, transmitted, and outputted to and from the Ethernet network in real time.

6

BRIEF DESCRIPTION OF THE DRAWINGS

The preferred embodiments of the present invention will be described with

5   reference to the following figures, wherein like numerals designate like elements, and

wherein:

Fig. 1 is an exemplary illustration of a system for uncompressed IP multimedia

data transmission and switching according to a preferred embodiment:

Fig. 2 is an exemplary illustration of an access device according to a preferred

10   embodiment;

Fig. 3 is an exemplary block diagram of an access device according to one

embodiment;

Fig. 4 is an exemplary block diagram of a coding module according to a preferred

embodiment;

15   Fig. 5 is an exemplary illustration of a flowchart outlining the operation of the

coding module according to a preferred embodiment;

Fig. 6 is an exemplary illustration of an access device according to another

embodiment;

Fig. 7 is an exemplary illustration of a decoding module according to a preferred

20   embodiment;

Fig. 8 is an exemplary flowchart outlining the operation of the decoding module;

Fig. 9 is an exemplary illustration of a digitized video signal;

Figs. 10a-10f are exemplary illustrations of video predictive coding and decoding

according to a preferred embodiment;

25   Fig. 11 is an exemplary illustration of a system utilizing data allocation according

to a preferred embodiment;

Fig. 12 is an exemplary flowchart outlining the operation of the allocation module

of the access device according to a preferred embodiment; and

Fig. 13 is an exemplary flowchart outlining the operation of a switch in response

30   to the allocation module of the access device according to a preferred embodiment.

<u>DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS</u>

Fig. 1 is an exemplary illustration of a system 100 for uncompressed IP

5   multimedia data transmission and switching according to a preferred embodiment. The

system 100 includes users 150, 160, 170 and 175, access devices 110, 120, 130, and 140,

and a network 180. Users 150, 160, 170 and 175 are users such as video/audio sources,

data terminals, video monitors, or the like. Network 180 is a network such as, a

Fast/Gigabit/10Gigabit Ethernet network, or the like. The system 100 provides for

10   interactivity between the access devices.

In operation, a user 150, such as a video camera, transmits multimedia data such

as composite video to the access device 110. The access device 110 reserves a channel

path across the network 180 during allocated bandwidth for channel allocation. The

15   access device 110 performs video predictive coding on the video signal and continuously

transmits the video in real time to another access device 140. The receiving access device

140 performs video predictive decoding on the video signal and outputs the data to a user

170 such as a video monitor.

20   Fig. 2 is an exemplary illustration of an access device 110 according to a preferred

embodiment. The access device includes ports 201 and 202, a coding module 210, a

decoding module 220, an allocation module 230, a network interface 240, and a user

input/output interface 250. The port 201 is a user port which receives or outputs a

multimedia signal and/or a video signal such a composite video signal. The network port

25   202 outputs the data to a network or receives data from a network such as a Fast Ethernet

network. The user port 201 is coupled to user input/output interface 250 which, in turn, is

coupled to the coding module 210, the decoding module 220, and/or the allocation

module 230. The network port 202 is coupled to the network interface module 240.

30   The coding module 210 is a video predictive coding module that performs video

predictive coding on an inputted video signal. In particular, the coding module 210 uses

8

the relationship between lines in a video signal to reduce the data content of the video signal before transmission to the network interface 240. Subsequent lines of the video signal can be recovered from current and previous lines and/or subsequent lines can be used to recover previous lines. For example, when a drastic change occurs between lines,

5   a subsequent line can be used to provide information to assist in recovering a line that encountered the drastic change. The decoding module 220 is a video predictive decoding module. The decoding module 220 performs video predictive decoding on a video predictive coded signal received from the network port 202. The allocation module 230 reserves a channel of the network 180 for transmitting the video predictive coded signal

10   according to the priority of the video predicted coded signal.

Fig. 3 is an exemplary block diagram of an access device 110 according to one embodiment. The access device 110 includes a video predictive coding module 210, an input interface 310, a delay module 320, a subtraction module 330, a timing control

15   module 340, a network interface 350, and a channel allocation module 230. In operation, the input interface 310 receives a video signal from the user port 201 (See Fig. 2). The delay module 320 delays a line of the video signal. The subtraction module 330 subtracts the subsequent line of the video signal from the delayed line of the video signal. The timing control module 340 controls the timing of the circuitry of the video predictive

20   coding module 210. The channel allocation module 230 reserves a channel of the Ethernet network for transmitting a video predictive coded signal according to a priority of the video predictive coded signal. The network interface 350 outputs the video predictive coded signal to the network 180. The video predictive coded signal is outputted in real time with reception of the video signal. In particular, the video

25   predictive coded signal is outputted substantially concurrently with the reception of the video signal. The video predictive coded signal can include a plurality of lines having a plurality of pixels.

Fig. 4 is an exemplary block diagram of a coding module 210 according to a

30   preferred embodiment. The coding module 210 includes DC restore circuitry 405, a synchronization separator 410, a phase lock loop clock generator 415, an analog to digital

9

converter 420, a line buffer 425, delay circuitry 430 and 435, line predictive coding circuitry 440, a buffer 445, and an Ethernet interface 450. In operation, the DC restore circuitry 405 conditions an analog video signal received from a video source from a port 201 (See Fig. 2). For example, the DC restore circuitry 405 conditions a video signal

5   received from a video camera. The synchronization separator 410 and the phase lock loop clock generator 415 act as timing control for the coding module 210. In particular, the synchronization separator 410 and the phase lock loop clock generator 415 control the timing of the video predictive coding module 210 for control synchronization or other synchronization purposes of the video predictive coding module 210. The analog to

10 digital converter 420 converts the video signal into a digitized video signal. The digitized video signal comprises multiple lines including multiple pixels. Each pixel can be represented by, for example, 8 bits of data to achieve 256 levels. The line buffer 425 creates a delayed line of the video signal. The delayed line of the video signal comprises a plurality of pixels. An undelayed line of the video signal enters the input buffer 430 of

15 the line predictive coding (or subtraction) circuit 440. A delayed line of the video signal enters the input buffer 435 of the line predictive coding (or subtraction) circuit 440. Input buffers 430 and 435 act as a buffer for the line predictive coding circuit 440. The line predictive coding circuitry 440 performs subtraction on the received digitized video signals. In particular, the line predictive coding circuitry 440 subtracts the digitized video

20 signal received from input buffer 430 from the delayed digitized video signal received from input buffer 435. Thus, the line predictive coding circuitry 440 subtracts a subsequent line of the video signal from a delayed line of the video signal. For example, if the original digitized video signal includes pixels of 8 bits each, the resulting transmitted video signal includes pixels of approximately 4 bits each. Thus, for example,

25 video can be transmitted in real time over a Fast Ethernet network because the resulting coded digitized video signal requires less than 100 Mb/s. In a preferred embodiment, a video signal can be transmitted in real time at a approximately 70-80 Mb/s. The buffer 445 is used to buffer the signal for output. The Ethernet interface 450 outputs the video predictive coded signal to an Ethernet network.

30

10

Fig. 5 is an exemplary illustration of a flowchart outlining the operation of the coding module 210 according to a preferred embodiment. The flowchart starts in step 510. In step 520, the coding module 210 receives a signal such as a multimedia signal. In particular, the coding module 210 receives a composite video signal. In step 530, the

5   coding module 210 performs video predictive coding on the received signal to create a video predictive coded signal. The video predictive coding is preferably done by delaying a line of the video signal and subtracting a subsequent line of the video signal from the delayed line of the video signal. Step 530 can include extracting a synchronization signal from the video signal to perform video predictive coding in

10   synchronization with the synchronization signal. Additionally, the video signal is converted from analog to digital in synchronization with the synchronization signal, and the video signal is buffered in synchronization with the synchronization signal. In step 540, the coding module 210 transmits the coded signal across the network, such as a Fast Ethernet network. The coded signal is transmitted substantially concurrently with

15   performing video predictive coding on the signal. In step 550 the flowchart returns to step 520. In a preferred embodiment, the resulting video predictive coded signal is represented by half the number of sampling bits per analog to digital sample point of the video signal.

20   Fig. 6 is an exemplary illustration of an access device 110 according to another embodiment. The access device 110 includes a video predictive decoding module 220, a network interface 610, a delay module 620, a subtraction module 630, a timing control module 640, and an output interface 650. The video predictive decoding module 220 includes the delay module 620 and the subtraction module 630. In operation, the network

25   interface 610 receives a video predictive coded signal from the network 180. The subtraction module 630 subtracts a subsequent line of the video predictive coded signal from a delayed line of the video predictive decoded signal. The delay module 620 delays a line of the video predictive decoded signal to create the delayed line. The timing control module 640 controls the timing of the circuitry for the output of the video

30   predictive decoding module 220. The output interface 650 outputs a video predictive decoded signal in real time to a user 170 such as a video monitor.

11

Fig. 7 is an exemplary illustration of a decoding module 220 according to a preferred embodiment. The decoding module 220 includes an Ethernet interface 705, a buffer 710, decoding circuitry 715, a line buffer 720, a clock generator 725, memory

5   control circuitry 730, frame buffer circuitry 735, and a digital to analog converter 740. In operation, the Ethernet interface 705 provides an interface for receiving a video predictive coded signal from the Ethernet network 180. The buffer 710 acts as a buffer for buffering the video predictive coded signal. The decoding circuitry 715 subtracts a line of the received video predictive coded signal from a delayed line of the video predictive

10   decoded signal. Line buffer 720 acts as a delay module for delaying a line of the video predictive decoded signal to create the delayed line of the video predictive decoded signal. The clock generator 725 and the memory control 730 act as synchronization circuitry to control the timing and synchronization of the frame buffer 735 and the digital to analog converter 740 in synchronization with the other circuitry. In particular, the

15   memory control circuitry 730 controls the frame buffer 735 and it can also be used for decoding when more than one line is used to recover a line being decoded. The frame buffer 735 buffers the decoded video signal. The digital to analog converter 740 converts the video predictive decoded signal into an output video signal for outputting to a user 170.

20

Fig. 8 is an exemplary flowchart outlining the operation of the decoding module 220. In step 810 the flowchart starts. In step 820, the decoding module 220 receives a signal such as a video predictive coded signal, such as, for example a video predictive coded video signal. The signal is received across an Ethernet network 180 from an access

25   device 110 utilizing a coding module 210. In step 830, the decoding module 220 performs video predictive decoding on the received video predictive coded signal to recover the video signal. Step 830 can include delaying a first line of the video predictive coded signal and subtracting a second line of the video predictive coded signal from the delayed first line of the video predictive coded signal to recover the video signal. Video

30   predictive decoding also includes extracting a synchronization signal from the video predictive coded signal so the signal is outputted in synchronization with the

synchronization signal. The signal is buffered and converted from digital to analog in synchronization with the synchronization signal. In step 840, the decoding module 220 outputs the decoded signal in a manner substantially concurrently with steps 820 and 830. In step 850, the flowchart loops back to step 820.

5

Fig. 9 is an exemplary illustration of a digitized video signal. The digitized video signal includes multiple lines A, B, C, etc. that include multiple pixels. For a composite video signal, each pixel includes 256 levels. Thus, each pixel can be represented by 8 bits.

10

Figs. 10a-10f are exemplary illustrations of video predictive coding and decoding according to a preferred embodiment. Coding circuitry can include delay circuitry 1010 and subtraction circuitry 1020. Decoding circuitry can include subtraction circuitry 1030 and delay circuitry 1040. In operation, a line A comprising pixels enters the coding

15 circuitry. The subtraction circuitry 1020 subtracts each pixel of the line from a line present in the delay circuitry 1010 (0 at this point). Next, the signal A is transmitted across an Ethernet network 180 and received by the decoding circuitry. The subtraction circuitry 1030 subtracts the received line A data from the line present in the delay circuitry 1040 (0 at this point). Then, as shown, in Fig. 10c, line A is present in the delay

20 circuitry 1010. Line B is subtracted from line A by subtraction circuitry 1020. The resulting signal is sent across a Fast Ethernet network and is received by decoding circuitry as illustrated in Fig. 10d. In Fig. 10d, the decoded line A is present in the delay circuitry 1040. The subtraction circuitry 1030 subtracts the received signal A-B from the delayed signal A to completely restore an output line B. Then, as shown in Fig. 10e, line

25 B is present in the delay circuitry 1010. Line C is subtracted from line B by subtraction circuitry 1020. The resulting signal is sent across a Fast Ethernet network and is received by decoding circuitry as illustrated in Fig. 10f. In Fig. 10f, the decoded line B is present in the delay circuitry 1040. The subtraction circuitry 1030 subtracts the received signal B-C from the delayed signal B to completely restore an output line C. Because the

30 difference of video line information (i.e., A-B, B-C, etc.) is sent, the number of bits representing the difference of a video line is statistically approximated to half of the bits

13

representing the video line without subtraction. In other words, if each video line pixel is represented by 8 bits, the average video line pixel after subtraction can be approximated by 4 bits.

5   Fig. 11 is an exemplary illustration of a system 1100 utilizing data allocation according to a preferred embodiment. The system includes access devices 110, 120, 130, and 140, a channel allocation priority packet 1110 including a payload 1120 and a header 1130, a master Ethernet switch 1140, and Ethernet switches 1150 and 1160. The access devices transmit multiple formats of data including packetized data and time-sensitive

10   data such as video data. The system 1100 reserves a portion of Ethernet bandwidth for real-time audio/video channel allocation. In particular, the system 1100 reserves a portion of Fast Ethernet 100 Mb/s for the channel allocation packet 1110. For example, the system 1100 reserves 100 kb/s for channel allocation packet 1110. The system 1100 operates like a circuit switched system, but not necessarily on a first come, first served

15   basis. For example, channel allocation can be based on the highest priority transmitted data or based on a chosen rule. For example, more important video data, such as security video, can take priority over lower priority video transmissions. The channel allocation priority packet 1110 includes a header 1130 addressed to the master switch 1140, and a payload 1120 that includes channel allocation priority data. For example, the channel

20   allocation priority data includes a priority code, priority definitions, or the like. The switches 1140, 1150 and 1160 are Fast Ethernet or faster Ethernet switches. The master switch 1140 receives the packet 1110 and reserves a channel path for high priority video data. The master switch 1140 reserves the path by allocating the path in the master switch and in slave switches such as switch 1150. Thus, time-sensitive data is

25   transmitted from the access device 110 to the access device 140 without interruption. The switches 1140 and 1150 thus block lower priority data. The system 1110 solves time-sensitivity problems encountered when transmitting time-sensitive data such as continuous video or multimedia data. The system 1110 assists in determining the priority of transmitted data. In particular, time-sensitive video data takes priority over packetized

30   data.

Fig. 12 is an exemplary flowchart 1200 outlining the operation of the allocation module 230 of the access device 110 according to a preferred embodiment. In step 1210 the flowchart begins. In step 1220, bandwidth is allocated by reserving a portion of Ethernet bandwidth for channel allocation. For example, 100 kb/s of 100Mb/s of Fast Ethernet bandwidth is reserved for channel allocation. In step 1230 a video signal is received that has an assigned channel allocation priority. The video can be a multimedia (audio/video/data) signal, a digital video signal, a composite video signal, or the like. In step 1240, the channel allocation priority is assigned to the video signal. In step 1250 the access device transmits the channel allocation priority to the master switch 1140 in the reserved portion of the bandwidth. In step 1260 the allocation module 230 receives a clear-to-send or delay-to-send signal form the master switch 1140. In step 1270, the allocation module transmits or delays the video signal based on the signal from the master switch 1140. In step 1280 the flowchart ends.

Fig. 13 is an exemplary flowchart 1300 outlining the operation of a master switch 1140 in response to the allocation module 230 of the access device 110 according to a preferred embodiment. In step 1310 the flowchart begins. In step 1320 a master switch 1140 receives a channel allocation priority packet 1110. The packet includes a header 1130 addressed to the master switch 1140 and a payload 1120 including channel allocation priority data. In step 1330, the master switch 1140 transmits a request-to-receive signal to the allocation module 230 of the access device 140. When a user at the access device 140 is ready to receive the video signal from the user at the access device 120, the allocation module 230 of the access device 140 sends a clear-to-receive signal back to the master switch 1140. In step 1340, the master switch reserves a channel path for the video signal to be sent by the access device 120, and transmits a clear-to-send signal to the allocation module 230 of the access device 120. In step 1350, when the master switch 1140 does not receive a clear-to-receive signal from the access device 140 in a pre-specified time interval or does not find an available channel path (based on the priority of the video signal) for the video signal to be sent by the access device 120, it issues delay-to-send signal to the allocation module 230 of the access device 120. In step 1360, the flowchart loops back to step 1320.

15

While this invention has been described with specific embodiments thereof, it is evident that many alternatives, modifications, and variations will be apparent to those skilled in the art. Accordingly, the preferred embodiments of the invention as set forth herein are intended to be illustrative, not limiting. Various changes may be made without departing from the spirit and scope of the invention.